

WHAT IS CLAIMED IS:

- 1 1. A caching system, comprising:
2 a tail FIFO memory having a tail input to receive incoming data and a tail output
3 to output the incoming data;
4 a memory having a memory input and a memory output, the memory input is
5 coupled to the tail output and the memory is operable to store the incoming data that is
6 output from the tail output, and wherein the memory is operable to output the stored data
7 at the memory output;
8 a multiplexer having first and second multiplexer inputs coupled to the tail output
9 and the memory output, respectively, the multiplexer having a control input to select one
10 of the multiplexer inputs to coupled to a multiplexer output;
11 a head FIFO memory having a head input coupled to the multiplexer output to
12 receive the incoming data, and a head output to output the incoming data; and
13 a controller coupled to the tail FIFO, the head FIFO, and the memory and
14 operable to transfer one or more blocks of the incoming data having a selected block size
15 from the tail FIFO to the memory and from the memory to the head FIFO, wherein the
16 selected block size provides a selected memory transfer efficiency level.
- 1 2. The system of claim 1, wherein the head FIFO further comprises a head
2 fill indicator coupled to the controller to indicate a fill characteristic of the head FIFO.
- 1 3. The system of claim 2, wherein the controller transfers the one or more
2 blocks of the incoming data having the selected block size from the tail FIFO to the
3 memory based on the head fill indicator.
- 1 4. The system of claim 2, wherein the controller transfers the one or more
2 blocks of the incoming data having the selected block size from the memory to the head
3 FIFO based on the head fill indicator.
- 1 5. The system of claim 1, wherein the tail FIFO further comprises a tail fill
2 indicator coupled to the controller to indicate a fill characteristic of the tail FIFO.

1 6. The system of claim 5, wherein the controller transfers the one or more
2 blocks of the incoming data having the selected block size from the tail FIFO to the
3 memory based on the tail fill indicator.

1 7. The system of claim 1, wherein the incoming data comprises data frames
2 of varying length and where the one or more blocks are defined to include data from one
3 or more of the data frames, and wherein a selected block may contain data from two or
4 more data frames.

1 8. The system of claim 1, wherein the controller includes a control output
2 coupled to the control input of the multiplexer, wherein the controller is operable to
3 control which of the multiplexer inputs is coupled to the multiplexer output.

1 9. The system of claim 1, wherein a data path to the memory is wider than a
2 width characteristic of the tail FIFO.

1 10. A method for implementing a caching system, the method comprising
2 steps of:
3 receiving data at a tail FIFO memory;
4 selecting an efficiency level for operating a memory interface;
5 determining a selected block size to support the efficiency level;
6 transferring one or more blocks of the data having the selected block size from the
7 tail FIFO memory to a head FIFO memory when the head FIFO is within a first fill level,
8 wherein the head FIFO memory includes an output to output the data;
9 transferring the one or more blocks of the data having the selected block size,
10 from the tail FIFO to a memory via the memory interface, when the head FIFO is within
11 a second fill level;
12 transferring the one or more blocks of data from the memory to the head FIFO
13 when the head FIFO is within a third fill level.

1 11. The method of claim 10, wherein the data comprises data frames of
2 varying length, and the method further comprises a step of defining the one or more
3 blocks of data having the selected block size to include data from one or more of the data

- 4 frames, and wherein a selected block of data may include data from two or more data
- 5 frames.

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